

forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/\text{cm}^3$ to $10 \times 10^{17}/\text{cm}^3$ at a temperature of 1000°C or higher to obtain a silicon epitaxial wafer; and

applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450°C to 750°C .

7. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the interstitial oxygen concentration is in a range of from $6 \times 10^{17}/\text{cm}^3$ to $10 \times 10^{17}/\text{cm}^3$.

8. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein the heat treatment temperature is in a range of from 500°C to 700°C .

9. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein the heat treatment temperature is in a range of from 500°C to 700°C .

10. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a substrate resistivity of the epitaxial wafer is $0.02 \Omega\text{-cm}$ or lower.

11. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a substrate resistivity of the epitaxial wafer is $0.02 \Omega\text{-cm}$ or lower.

12. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω -cm or lower.

13. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω -cm or lower.

14. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

15. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 7, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

16. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 8, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

17. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 9, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.

18. (Added) The manufacturing process for a silicon epitaxial wafer according to claim 10, wherein a dopant in a substrate of the silicon epitaxial wafer is boron, arsenic or antimony.